MICROMACHINED STIMULATING ELECTRODES

Quarterly Report #7

(Contract NIH-NINDS-N01-NS-5-2335)

April 1997 ---June 1997

Submitted to the

Neural Prosthesis Program
National Institute of Neurological Disorders and Stroke
National Institutes of Health

by the

Center for Integrated Sensors and Circuits
Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, Michigan
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Summary

During the past quarter, additional passive stimulating and recording probes have been fabricated for use by investigators nationwide. A new mask set was also prepared to test a variety of site structures fabricated using two and three mask processes. Wafers are now in process to determine the yield and structural integrity of these sites in an effort to standardize on a design that will offer maximum reliability and yield in future probe fabrication. A new sectioning/polishing technique has been developed to allow cross-sections to be obtained at high resolution through these sites so that they can be evaluated in ways not previously possible. Test structures have also been included to allow the optimization of beam lead dimensions and the bonding parameters associated with these lead transfers.

As part of the continuing optimization of the probe process, we are exploring two new technologies that could offer alternatives, or supplemental processes, to the boron diffusion process now used for probe fabrication. Deep high-aspect-ratio dry etching technology now permits aspect ratios of more than 30:1 and could be used to trench around probe patterns to speed, for example, shank etchout (in combination with a boron etch-stop). Sometimes in the past the shanks have cleared too slowly, delaying etch termination and resulting in excessive attack of circuit areas on active probes. A porous silicon process is also being explored. This electrochemical technique allows formation of a very fast etching layer under normal circuit material and could allow an etch-stop to be formed under lightly-doped silicon containing the circuitry at the back of a probe. This would eliminate any critical timing windows in the formation of active probes. Probes are in process using this porous silicon technique.

Active stimulating probes STIM-2B and -3B are continuing in fabrication. New masking techniques for forming the spacer slots on active 3D structures have been verified experimentally as have layout changes to minimize or eliminate lateral attack of the circuit areas on active probes. These layout changes and the associated etching studies have greatly added to our understanding and ability to optimize the process windows associated with 3D active probe fabrication. We expect completed versions of these active probes during the coming quarter along with the new version of external circuitry for interfacing with them.

MICROMACHINED STIMULATING ELECTRODES

1. Introduction

The goal of this research is the development of active multichannel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highly-controlled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully and distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data which can be demultiplexed on the probe to provide access to a large number of stimulating sites. Our goal in this area has been to develop a family of active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into per-channel current amplitudes which are then applied to the tissue through the sites. Such probes generally require five external leads, virtually independent of the number of sites used. As discussed in our previous reports, we are now developing a series of active probes containing CMOS signal processing electronics. Two of these probes are slightly redesigned versions of an earlier first-generation set of designs and are designated as STIM-1A and STIM-1B. A third probe, STIM-2, is a second-generation version of our high-end first-generation design, STIM-1. All three probes provide 8-bit resolution in digitally setting the per-channel current amplitudes. STIM-1A and -1B offer a biphasic range using ±5V supplies from 0μA to ±254μA with a resolution of 2μA, while STIM-2 has a range from 0 to ±127μA with a resolution of 1μA. STIM-2 offers the ability to select 8 of 64 electrode sites and to drive these sites independently and in parallel, while STIM-1A allows only 2 of 16 sites to be active at a time (bipolar operation). STIM-1B is a monopolar probe, which allows the user to guide an externally-provided current to any one of 16 sites as selected by the digital input address. The high-end STIM-2 contains provisions for numerous safety checks and for features such as remote impedance testing in addition to its normal operating modes. It also offers the option of being able to record from any one of the selected sites in addition to stimulation. It will be the backbone of a multi-probe three-dimensional 1024-site array now in development. A new probe, STIM-2B, is currently being added to this set. It offers 64-site capability with off-chip generation of the stimulus currents on four separate channels.

During the past quarter, we have continued to fabricate passive probe structures for internal and external users. Wafers are being fabricated with three different stimulating site structures in order to define the most reliable process for these areas. A sectioning/

polishing technique has been developed to allow the sites to be explored in detail. Probe process enhancements are being explored for active probes, including the use of deep dry etching and the use of porous silicon sacrificial layers. Finally, STIM-2B/3B are in fabrication. Masking/layout changes have resulted in much greater protectiuon for the on-chip circuitry while ensuring that the slots and wings on the 3D structures can be formed reliably. The results in each of these areas are described more fully in the sections below.

2. Passive Probe Developments

Fabrication and distribution of passive probes under the Center for Neural Communication Technology continues. During the past quarter, a second run of CNCT3 was completed. This layout includes designs submitted by Drs. Bill Heetderks and Edward Schmidt of the NIH, Dr. Gyorgy Buzsaki of Rutgers, and Dr. Steven Highstein of Washington University.

The probe designed by Drs. Heetderks and Schmidt is shown in Fig. 1. This probe, intended for visual cortex stimulation studies, has one site on each of its two shanks. It is designed to mimic the wire device used in their current cortical studies. A platform was also designed so that the device can rest on the surface of the cortex similar to our 3-D arrays. A breakoff tab was included at the top of the probe to aid in handling during packaging.

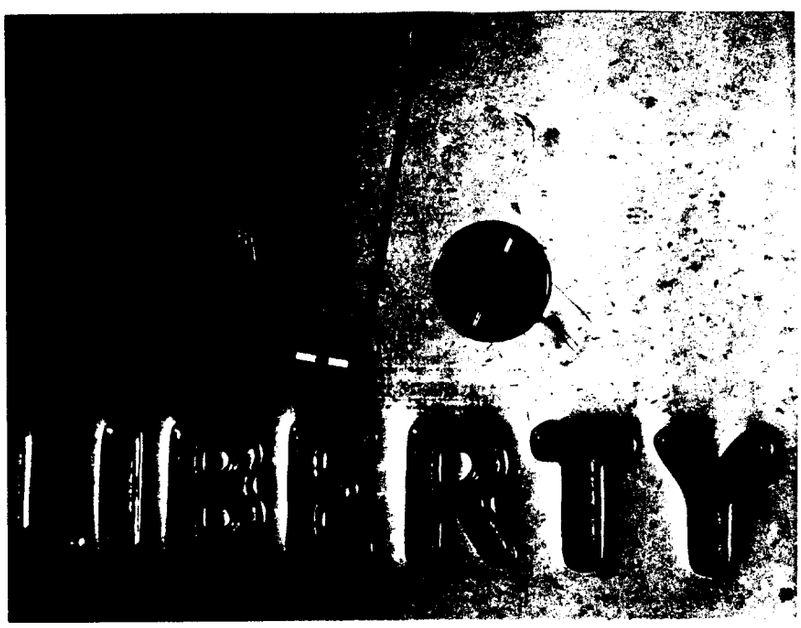


Fig. 1: Stimulation probe designed by Drs. Heetderks and Schmidt. The probe is designed for use in visual cortex. The companion platform has slots to accept the probe shanks which are spaced at 500μm.

Dr. Buzsaki designed several probes to be used as tetrodes in his hippocampal studies. As shown in Fig. 2, we fabricated mirror images of the probes, which will permit them to be placed in very close proximity to one another on separate connectors. Separate connectors will permit the probes to be moved independently throughout the experiment.

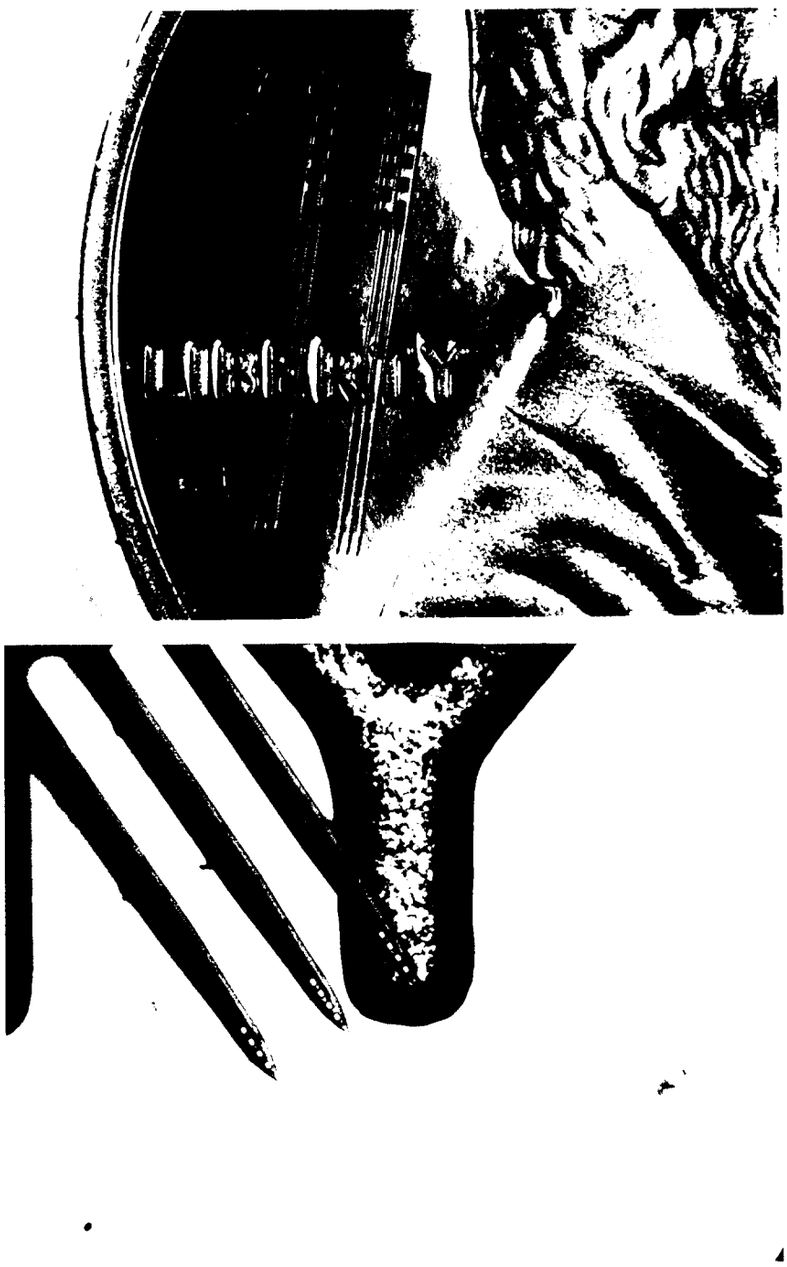


Fig. 2: Recording tetrodes designed by Dr. Buzsaki. Mirror images of the probes were designed to be placed in close proximity to one another on separate connectors, permitting them to be moved independently of one another. On this particular design, each shank has four sites spaced at 25µm. The shanks are on 150µm centers.

Dr. Highstein continues his work with sieve electrodes for recording from regenerating vestibular nerve fibers in the toadfish. One of the designs which he included on CNCT3 is shown in Fig. 3. This particular probe has 8μm diameter holes, nine of which are outfitted with annular recording sites.

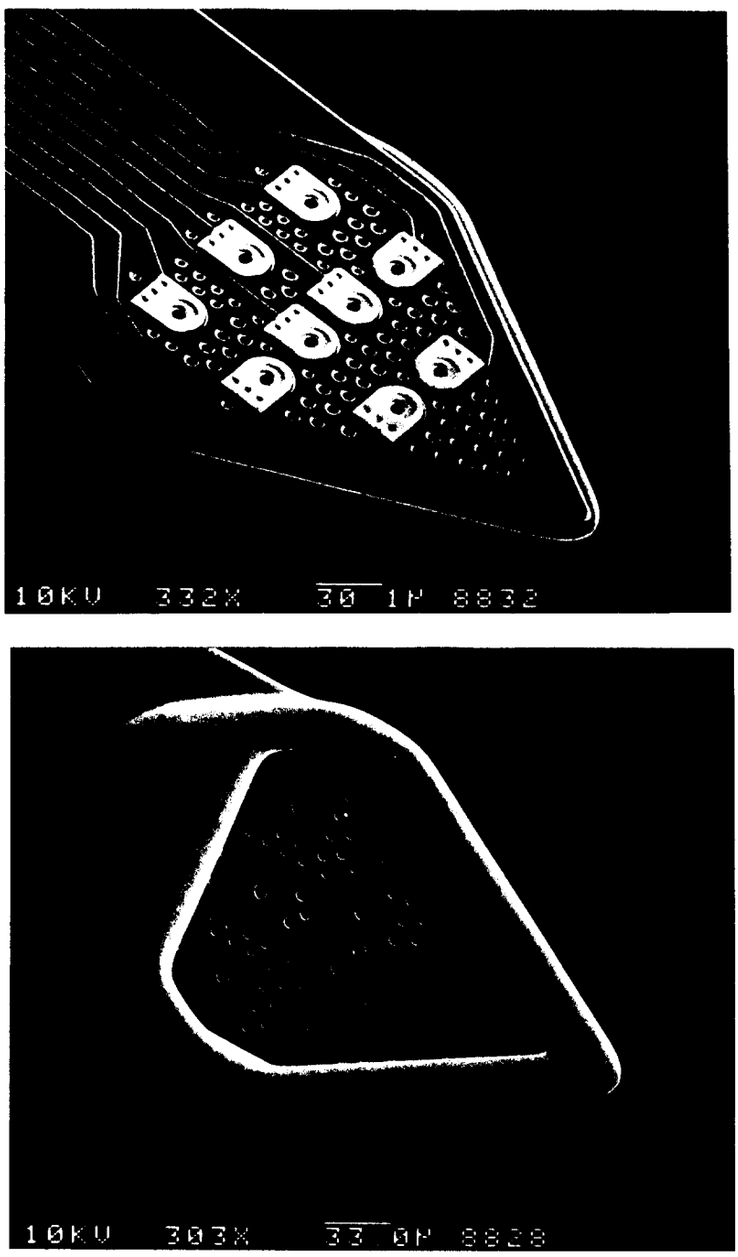


Fig. 3: Sieve electrode designed by Dr. Highstein. As shown by the back view of this device, the main structure is a dielectric membrane which is supported by an outer deep boron doped ring. The widest dimension of this device is 175μm. Nine of the 8μm holes are outfitted with annular recording sites.

Site Formation

Although this subject is typically covered in the recording report, it is pertinent to both contracts and will therefore be updated here. Problems with reliable contact formation have been described in detail previously and will not be repeated here. In general, these problems have been attributed to a number of causes, including polymer formation in the contact openings and poor step coverage of the metal. In the most recent recording report, ("Thin-film Intracortical Recording Microelectrodes" QR #1, May 1997), we detailed four methods for site formation (see Fig. 4) along with their associated advantages and disadvantages. Since that time, a mask has been designed to test methods 2, 3 and 4 and it is currently being processed.

The layout includes typical recording and stimulation probes for electrochemical evaluation, and various test structures for use in SEM analysis and electrical testing on the probe station. While all three methods can be tested using the same masks, it will not be possible to include the three methods on a single wafer. This would have required additional masks and processing steps. However, all wafers are being subjected to the same furnace, RIE, and sputtering runs so that the methods can be directly compared.

In conjunction with the site study, we have been evaluating a polishing technique for its utility in SEM analysis of sputtering coverage in contact openings. While top-view micrographs of contact openings can reveal possible problems (see Fig. 4, "Thin-film Intracortical Recording Microelectrodes" QR #1, May 1997), cross-sections should result in more definitive conclusions. Polishing permits an exact cross-section of a contact to be realized as opposed to attempting to break off a shank and hitting a contact by chance. Precise breaks are quite difficult as contact openings can be as small as 3μm. There is also a chance that the breakage may confound the results due to jagged edges. The polishing process involves mounting the probe specimen onto a small tripod device. Diamond films, varying in grain size, are used to grind away the silicon until the desired location is reached. The probe is then removed and the cross-section is viewed with the SEM. Figure 5 shows an example of a contact cross-section viewed using this technique. One of the test structures included on the new mask has sites with 500μm-long contact openings which should make the polishing technique even simpler.

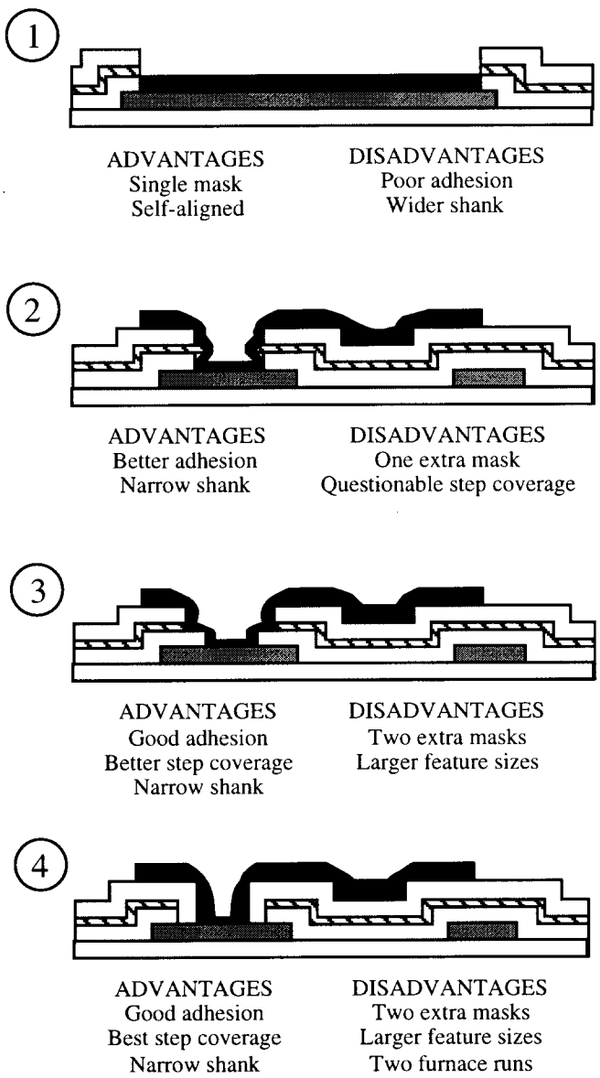


Fig. 4: Four options for electrode site formation. The first is a single mask, self-aligned process. The second requires two masks but has the added advantage of inclusion of an intermediate cleaning step. The third and fourth methods require yet another mask (three in total) but are more foolproof in terms of step-coverage.

We have included one final test structure on the new mask in an effort to optimize dimensions of our beam leads for maximum bond strength. This is an important issue since all of our 3-D assemblies require beam leads for electrical contact between the probes and the platform and there is some concern that the current beam leads are too wide. This two-piece test structure, shown in Fig. 6, has beam leads ranging in width from 25μm to 75μm. A hole through one side of the structure will permit utilization of a hand scale for quantitative comparison of the forces required to break a bond. Thus, using this simple mask set we should be able to optimize beam dimensions and bonding parameters to ensure reliable lead transfers. Pull tests will quantify bond strength as a function of these parameters.

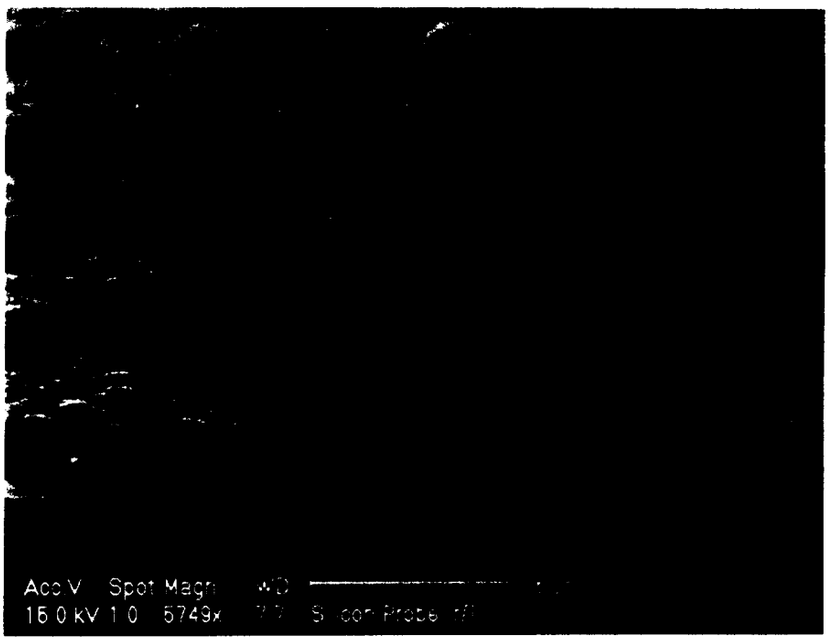


Fig. 5: SEM of an iridium site with multiple 3µm contact vias. This cross-section was formed using a polishing technique which recently became available to us. Precise views of contact openings such as this should permit a more accurate evaluation of sputtering coverage for the three site formation methods.

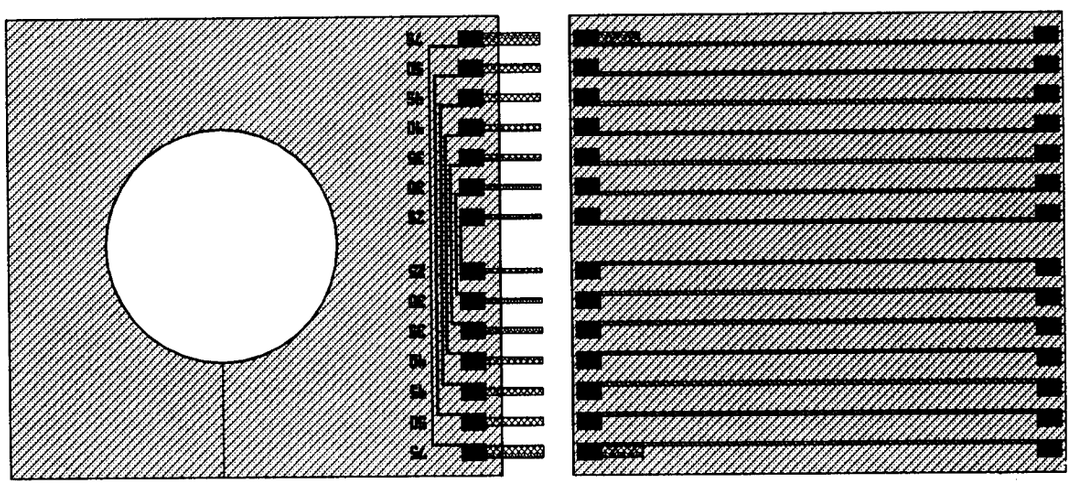


Fig. 6: Test structure for evaluation of beam lead strength. The hole will permit utilization of a hand scale to quantify forces necessary to break a bond.

3. *New Micromachining Process Development*

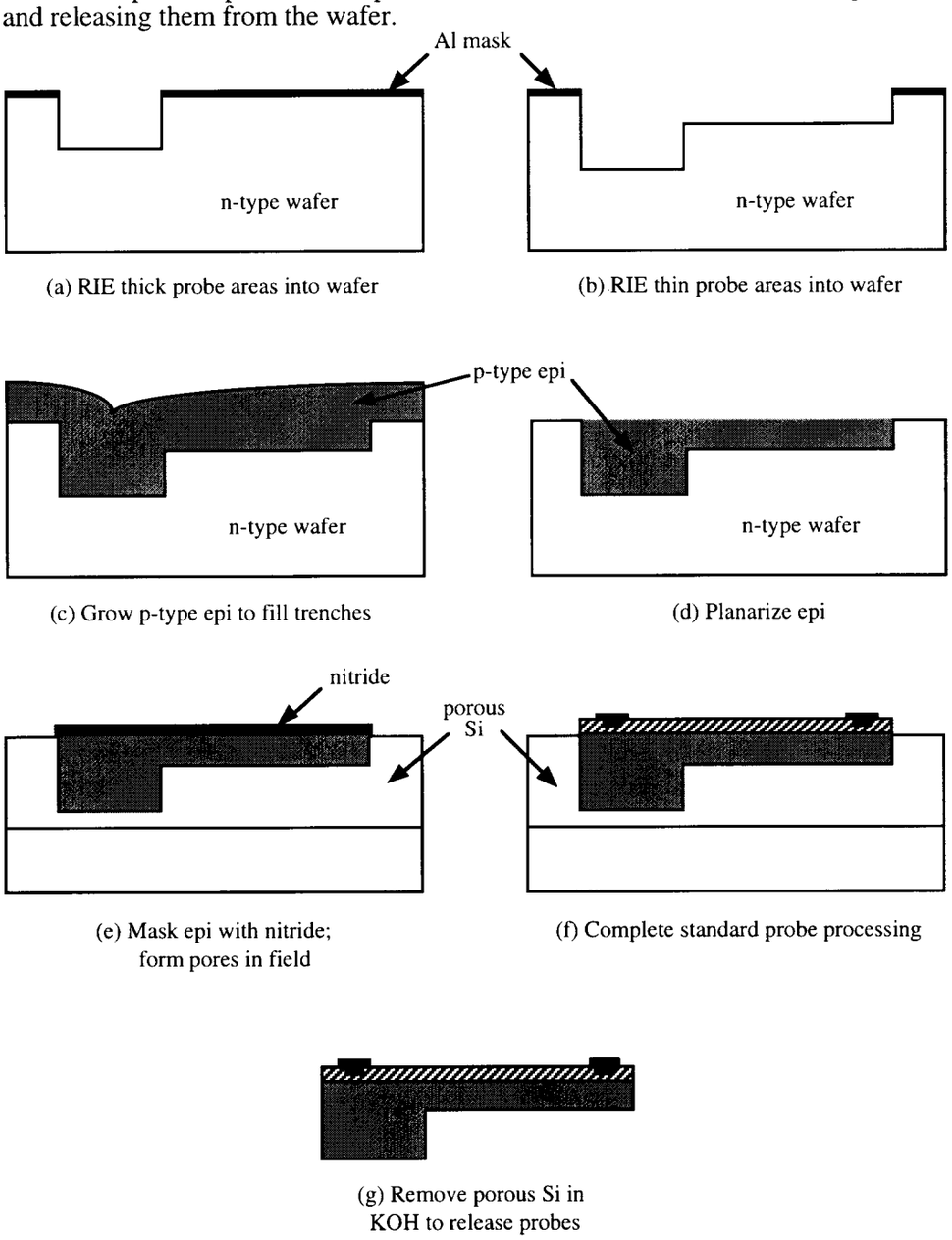
A key step in the formation of all of the neural probes we have been pursuing is the use of a high-concentration boron diffusion to form the probe shape. This works well and has allowed probes to be scaled down to widths as small as 5μm. However, the diffusion process is less standard in industry today than it was twenty years ago. As integrated circuits have become denser and shallower, diffusion has been replaced by ion implantation; however, for our deep boron diffusions, the dopant doses required are so high as to preclude ion implant as a practical doping method. Thus, the deep boron processing step is one that must be dealt with as we transfer the probes to commercial/foundry production. To date, in those probes not made entirely in-house, we have nonetheless performed the boron diffusions in-house along with site metallization, with the remainder of the process run externally (e.g., at MCNC). A few commercial process foundries are now offering the deep boron process, however, and its use is not uncommon in MEMS devices, especially in larger companies (e.g., in GM, Ford, Rockewell, and elsewhere). In our active probe process, there is also the problem of stopping the wafer dissolution etch over the circuit area of the probe, where there is no formal etch-stop employed. While for 2D structures, there is an acceptable process window here, the situation is more complicated in 3D active structures, where lead-transfer wings must be formed from boron-doped silicon while thicker silicon nearby must be retained for the circuit areas. This problem is discussed further in the next section.

As we continue probe development, we need to be constantly aware of new technologies that could offer advantages over our current approaches to probe formation. So far, we have found none that offer, overall, advantages over the boron process; however, two technologies have recently emerged that may offer alternatives, or supplements, to the use of deep boron diffusions. These are 1) deep high-aspect ratio dry etching, in which slots 100μm deep can be formed rapidly in silicon with aspect ratios greater than 30:1, and 2) porous silicon processes, in which fast-etching layers can be formed electrochemically in the silicon bulk. Both technologies are now being explored for use with, or in place of, our normal boron doping. Deep etching may offer additional help, used with boron doping, in getting shanks and wings to etch out prior to the circuit areas to increase the available process window in probe fabrication. Porous silicon could offer a replacement for boron diffusions altogether, or at least for use under the circuit areas of the probe.

Porous silicon is formed by the anodic etching of silicon in hydrofluoric (HF) acid. Although silicon is not normally attacked by HF, placing a positive bias on a silicon sample relative to an HF solution in which it is immersed results in the formation of pores in the silicon. Due to its extremely high surface-to-volume ratio, the porous material can be removed in a silicon etchant, such as KOH, in such a short time that surrounding non-porous silicon is essentially untouched. This makes it an ideal material for use as a sacrificial layer. The formation of pores in silicon is selective with respect to dopant type and concentration of the substrate, which allows dopant junctions to be used as etch-stops when forming pores.

A proposed process flow which uses porous silicon to micromachine neural probes is illustrated in Fig. 7. The thick (currently deep-boron) probe substrate areas are dry etched (recessed) into an n-type wafer substrate. The same method is then used to define the thin (currently shallow boron) probe substrate areas. Next, the recesses are filled with p-type epitaxial silicon, which forms the probe substrates. The epitaxial silicon (epi) is mechanically polished to remove it from the field and planarize the wafer. The probes are

then covered with nitride to mask the formation of pores in the epi, and the wafer is anodically etched, forming pores in the field. The pn-junction at the side and bottom surfaces of the probes acts as an etch-stop which keeps the formation of pores on the field side of the junction. Since pore formation is an isotropic process, pores form laterally as well as vertically, undercutting the probes. All remaining processing can then be performed as is now done on top of the porous layer to complete the probe fabrication. As the final step in the process, the porous silicon is removed in KOH, lifting out the probes and releasing them from the wafer.



(a) RIE thick probe areas into wafer

(b) RIE thin probe areas into wafer

(c) Grow p-type epi to fill trenches

(d) Planarize epi

(e) Mask epi with nitride; form pores in field

(f) Complete standard probe processing

(g) Remove porous Si in KOH to release probes

Fig. 7: A process flow for fabricating neural probes using a porous silicon sacrificial layer as the micromachining tool.

We are currently working on a passive probe run using this process flow, as well as doing extensive characterization of the pore formation process. Figure 8 is an SEM photograph showing the cross-section of the bottom of a porous layer formed in n-type silicon. In Fig. 9, a dopant junction etch-stop and the lateral formation of pores are demonstrated. Here pores have been formed in an n-type wafer, undercutting a p-type diffused area which has been masked on top with nitride.

This porous-silicon probe formation process has advantages in the production of active probe structures since the etch rate in the sacrificial porous layer is so high that there is essentially an etch stop around the circuitry. The porous silicon can be etched in KOH only slightly above room temperature, where its etch rates in normal bulk silicon and in dielectrics is negligible. High-concentration boron diffusions are not required, and all of the processes used are relatively common in the production of current integrated circuits. However, overall this process is also more complex and a good deal more difficult than our normal diffused-boron process. It uses epitaxy, chemical-mechanical planarization (CMP), and the biased creation of the porous layer, all of which are relatively advanced processes. Thus, the question of whether this approach offers significant advantages over a boron diffusion is not clear. We are fabricating probes using porous silicon so the process can be compared with our more standard diffusion process. In this way, we hope to ensure that we are doing things the best way in terms of running a process that will have the maximum impact on the neurosciences.

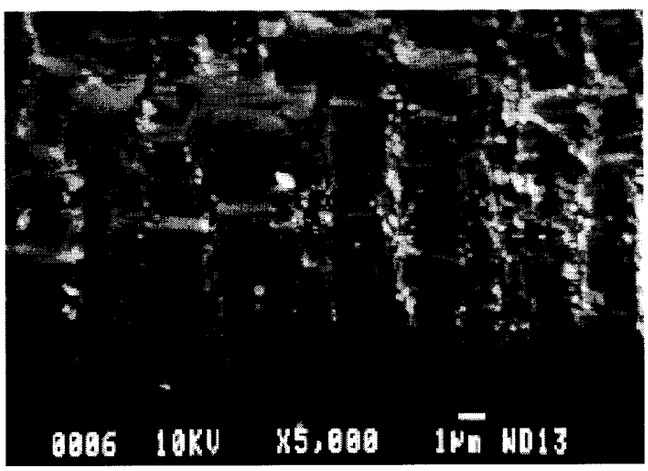


Fig. 8: An SEM photograph of pores formed by the anodic etching of n-type silicon in HF acid.

4. Active Stimulating Probe Development

During the past quarter, work on the active stimulating probe project has primarily focused on the fabrication of the STIM-2B/STIM-3B probe set. Etch-out tests were also performed on the designs to ensure that the probes, namely the shanks, wings and slots, would etch out properly while still providing protection for the back-end circuit area. A special technique, utilizing the anisotropic etching characteristics of ethylenediamine-pyrocatechol (EDP), was used in the layout of the entire wafer mask such that all of the circuit corners were protected from attack by the final release etch in EDP. The tests showed that the technique used was quite successful.

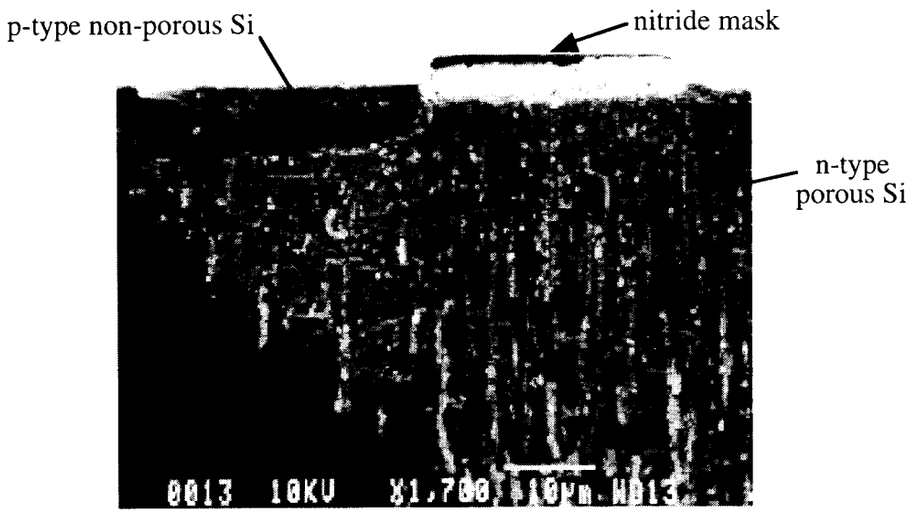


Fig. 9: An SEM photograph of pores formed in an n-type substrate undercutting a p-type diffused area. The pn-junction prevents the formation of pores in the p-type area.

STIM-2B

The second-generation four-channel 64-site version of the simplest active stimulating probe, STIM-2B, is currently in fabrication. This design utilizes a 20b shift register to load four 4b site addresses which are decoded by a 1-of-16 decoder to connect the designated site to an analog input/output pad through a large CMOS passgate transistor. This allows 'steering' of externally generated currents to the addressed site. A fifth bit is included along with the 4b site address in order to select between the stimulation and a newly added recording function. The fifth bit simply selects either a direct path between the I/O pad and the site or selects the path through an amplifier for recording from the same site.

The most important feature of this design is the fact that the probe is almost completely digital. The only analog portions of STIM-2B are the amplifiers. The design is such that if the amplifiers do not function as expected due to bias changes caused by process variations, the probe will still function normally for stimulation. The digital nature of STIM-2B lends itself to a very robust design.

STIM-3B

The extension of the STIM-2B probe, a 2-D probe, to a 3-D probe has been referred to as STIM-3B. The changes essentially involve some structural changes in the probe geometry to accommodate assembly and connection with a platform assembly and a few circuit enhancements which are necessary to allow addressing of multiple probes.

The structural changes needed are simply to include the wings and beam-lead interconnects for assembly and lead transfer from the individual probes to the 3-D platform. As discussed in the previous report, 45° angled slots were incorporated into the wing to

ensure that the wings would etch clear so that the spacers of the 3-D assembly would properly fit down over them. The angled slots allow a continuous trench to be etched from the front side of the probe even before the etch plane advances from the backside during the final release etch in EDP. The integrity of the circuitry is ensured by making sure the surrounding deep boron diffused rim is wide enough so that the lateral undercut from the corners does not have time to reach the active circuit area. As mentioned previously, a new technique for protecting the circuitry was included at the full wafer layout level. Both methods were included because the second method was as yet an unproven method. This new method and the test results will be discussed more in depth later. Figure 10 shows the overall layout of the STIM-2B/3B mask set.

The circuit changes necessary to realize a 3-D probe were kept to a minimum in order to maintain probe simplicity while still resulting a flexible 3-D system. An additional 4b shift register was included with each bit used as a flag bit to select/deselect an I/O line via a large CMOS passgate placed in the line. The last bit of the 4b shift register would also be buffered out onto an additional lead to go off probe. The operation of the complete 3-D system is then quite simple. All of the probes in the array share common analog I/O data lines, power lines, clock lines and y-addr (normal probe address) lines. The same y-addr is clocked into the 20b shift register on all the probes. The key feature is that while the y-addr is being clocked into all the probes, an x-addr (I/O channel enable) is simultaneously being clocked into the first probe and daisy-chained to the second, third, and nth probe via interconnecting leads on the platform thus making an extended 'virtual register'. Differing numbers of probes in the array would result in differing x-addr lengths, but it would only be necessary to be sure that the last bits of both the y-addr and x-addr arrived at the same time. For example, for a 4 probe system, the y-addr would be 20b long as always, but the x-addr would only be 16b long. This means that the actually x-addr data would not begin until the fifth clock time slot. Theoretically, the size of the array is unlimited because probes can be daisy-chained together indefinitely. Practically, the array would simply get too large and as the number of probes goes beyond 5, the time necessary to enter a new set of addresses also increases as the limiting address length becomes the x-addr when it passes 20b.

This results in a system with ten leads that can select almost any combination of four channels across the array. The design allows for a variable/expandable array size which can be determined by simply having a different platform configuration. This design also allows inter-probe stimulation. One weakness is the fact that the same probe I/O channel cannot be simultaneously driven with an independent stimulus current. If the same channel were selected on more than one probe, the stimulus current would be shared between the probes because of the bus type of connection. Given the tradeoffs between flexibility and simplicity, this design was chosen because it is fairly flexible without a great increase in complexity. There were some additional fabrication issues that were addressed in relation to this new set of probes and to the problem of successfully realizing active probes, in general, with a dissolved wafer process while maintaining circuit integrity. The first problem specific to STIM-3B (and any future 3-D designs) is that of protecting the active circuit area from being undercut during the final EDP release etch, while at the same time ensuring that the platform mounting wings of the 3-D probe structure are completely etched clear so that the spacers can properly fit down over them. As discussed in the previous report, this problem was addressed by opening 45° angled slots in the area which the spacer must slide down over. These slots allow a continuous trench to be etched from the front side of the probe even before the etch plane advances from the backside during the final release etch in EDP. Etch tests, which will be discussed later, have shown this to be a very successful method.

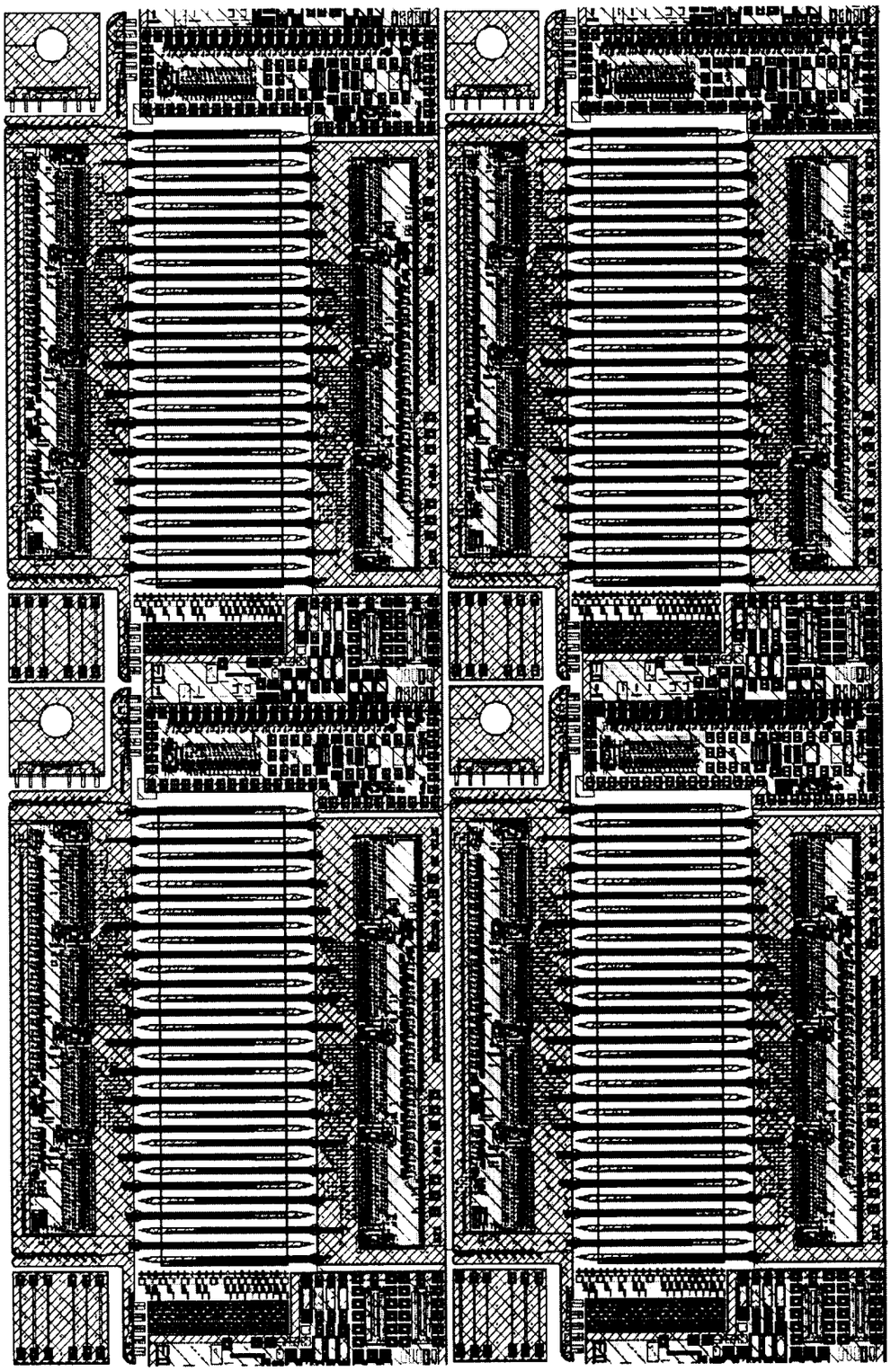


Fig. 10: Overall layout of the STIM-2B/3B mask set. The chip area shown contains four STIM-2B and four STIM-3B probes plus a number of process and circuit test blocks.

The second, more general, problem is that of protecting the circuitry from being attacked by the lateral undercutting from the front side of the wafer during the final etch. One method is obviously to simply increase the width of the deep boron ring around the circuitry. The problem with this is that it significantly increases the size of the probe and still does not always provide the desired protection. A new technique to protect the circuitry has been included on this mask layout to see if it could be used such that the deep boron ring could be made narrower. The new technique simply utilizes the etching characteristics of EDP in that the etch rate in the <100> direction is much higher than that in the <111> plane. The etch virtually stops on the <111> plane, although there is still a finite etch rate. This characteristic is used to create trenches around the circuit area on the front of the wafer ("V-grooves") to a depth that can be defined by the width of the mask opening in the field etch mask. In order to stop the etch from continuing to etch under any corners, a small bridge of field dielectric is left there so that the trench must terminate at the bridge. This eliminates any outside corners on the mask pattern and the associated undercutting that would occur there. Figure 11 demonstrates how two of the bridges are used to protect the corners of two adjacent probes in the layout. Figure 11 is a blow-up of area 1 of Fig. 12. The bridges are designed to taper down to a very narrow width of 7μm. The reason for this is so that the bridge is easily etched away when the etching plane from the backside of the wafer breaks through into the bottom of the frontside formed trenches. Once the backside etch breaks through into the bottom of the trench, the agitation of the EDP etch begins to break the probes apart and the is completed. If the bridges were made wider, the probes could also be kept in a wafer frame so that they could be snapped apart later. Unless the shanks can be undercut from the from side, which is not likely due to their length, the separation between the shanks, which are interleaved in the wafer level layout, must be greater than the trench opening around the circuit area. This is necessary so that the trench formed between the shanks is deep enough that the back etch breaks through more quickly than the circuit trenches thus allowing the shanks to be etched clear from the backside. A deep dry etching trench could also be used to accelerate shank etch-out.

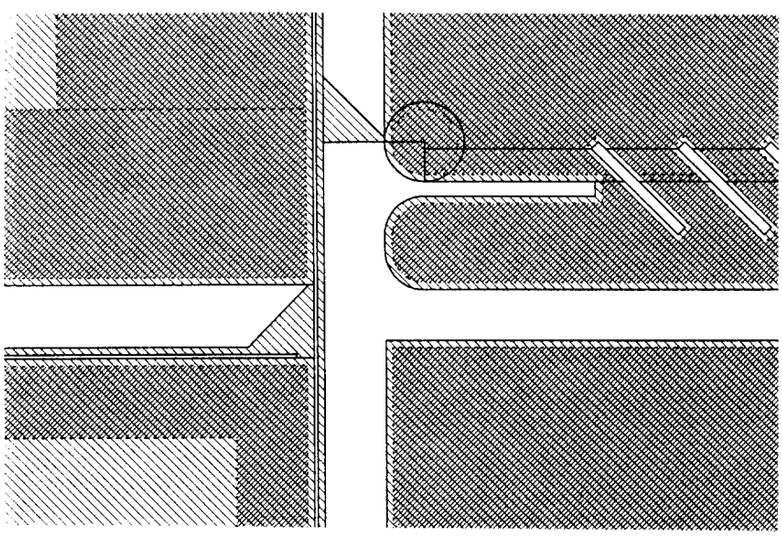


Fig. 11: A blow-up of area 1 of Fig. 12. This shows the layout of the bridged corner protection technique near the wing area of a STIM-3B probe in the wafer level layout.

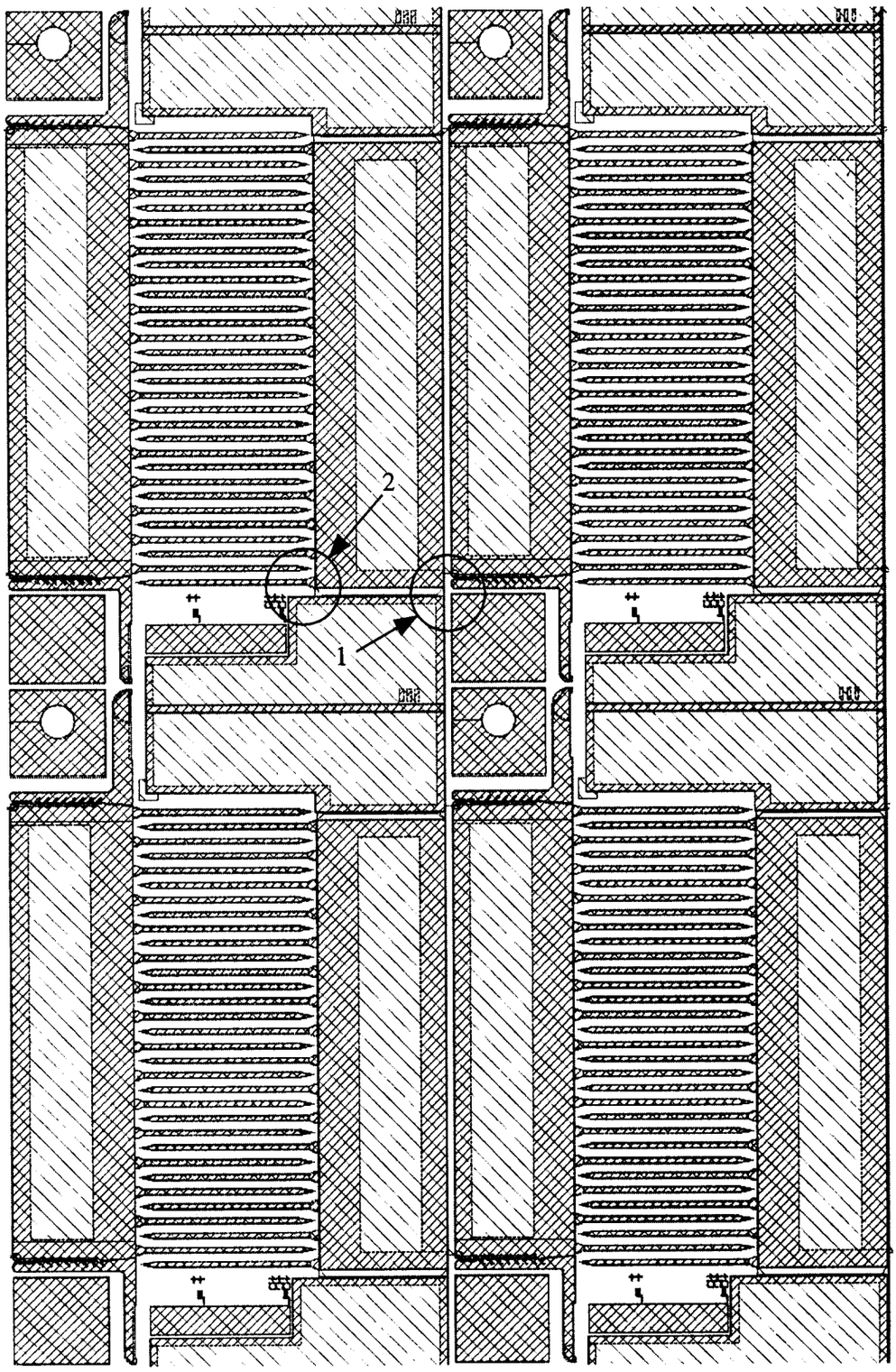


Fig. 12: The layout of four adjacent cells at the wafer layout. A blow-up of area 1 is shown in Fig. 11. A blow up of area 2 is shown in Fig. 17.

ETCH-OUT TESTS

Several wafers were processed using only one and/or two of the masks from the current mask set: the deep boron mask and the final field dielectric etch mask. A sample wafer was fabricated by growing 1.3μm of thermal oxide and then patterning the oxide with the final field etch mask using a wet etch. The wafer was then quartered and the four quarters were each etched for different amounts of time: 20, 40, 60, and 80 minutes. This allowed us to see progression of the *frontside-only* etch (the wafer backside is protected by the dielectric) since the dielectric is clear and we could see the underlying silicon easily with a light microscope. The progression of the etch in the area shown in Fig. 11 is shown in Figs. 13-16. The progression shows that the bridges do indeed do a good job of protecting the circuit area from being undercut from the frontside etching. After an hour and 20 minutes the bridges have been etched away, but minimal undercutting has occurred. It should be pointed out that due to the isotropic nature of wet etching as used in the oxide mask etch, the dielectric the bridges were only about 4μm wide as opposed to 6-7μm as they will be when etched out with an anisotropic dry etch as will be used in the actual probe processing. It is also noted that the angled slots allow the spacer area to undercut quite quickly.

The manner in which the probe shanks etch out is also important in how the final release etch will perform. Figure 17 shows a blow-up of area 2 in the Fig. 12 layout. This is the area that is shown in the series of pictures of Figs. 18-21 which are from the same etching samples as the previous series of pictures. The most important thing to note is that the shanks do undercut from the front-side, but due to the alignment the shanks only undercut from the tip. This would obviously take too long; therefore, it is necessary that the backside etch complete the etch-out. This will occur when the backside etch plane meets the trenches formed between the shanks. Once that occurs the etch very rapidly attacks the exposed corners clearing the shanks very rapidly.

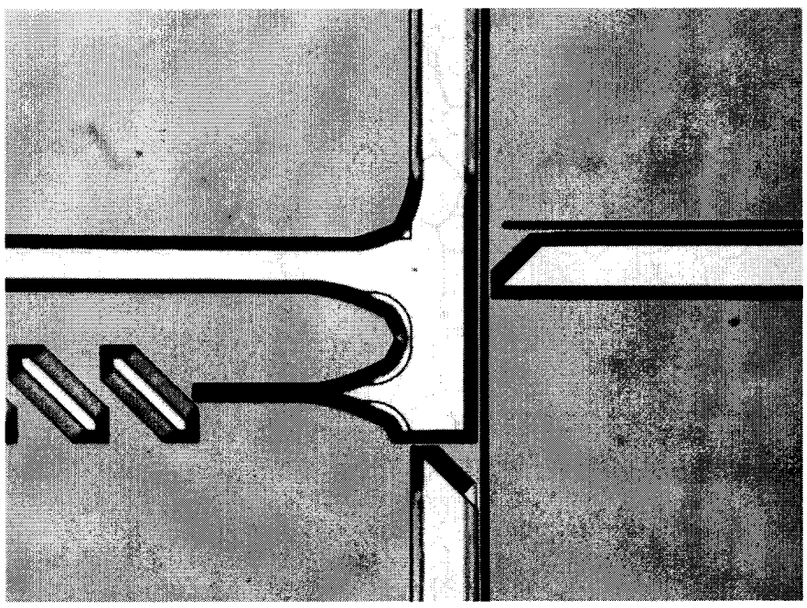


Fig. 13: The EDP etch progression in the same layout area as Fig. 11 after 20 minutes; the angled slots begin to etch out and trenches begin to form around the back of the circuit areas.

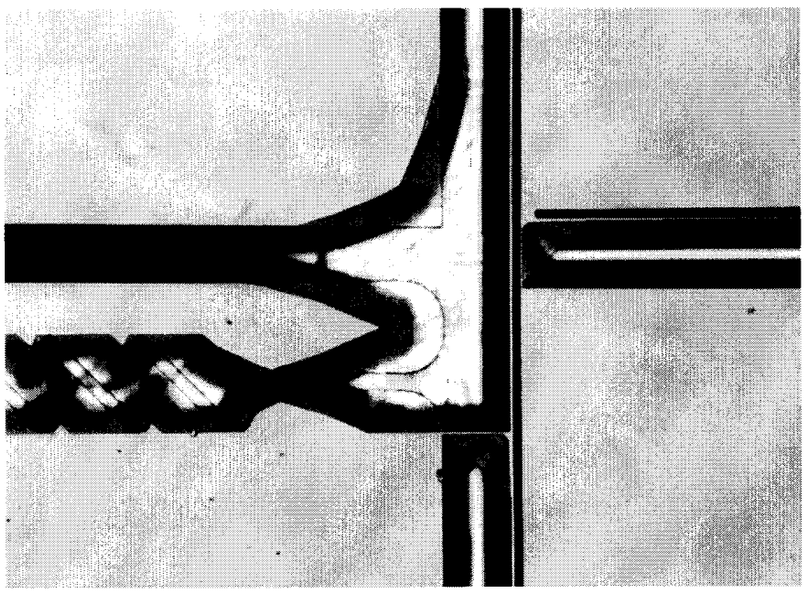


Fig. 14: The EDP etch progression in the same layout area as Fig. 11 after 40 minutes; the angled slots have almost formed a complete trench in the spacer slot area and the circuit area trenches continue to deepen.

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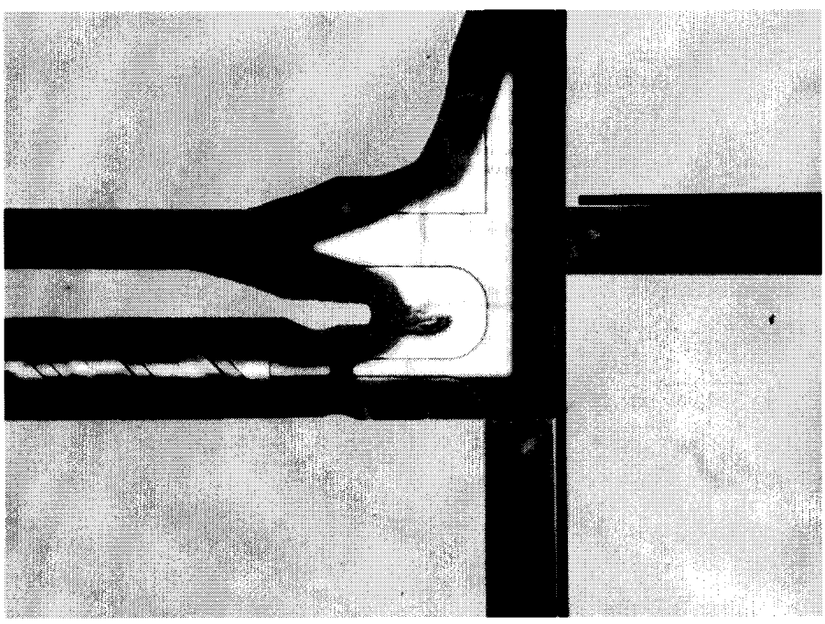

Fig. 15: The EDP etch progression in the same layout area as Fig. 11 after 60 minutes; the spacer trench is nearly complete. The corner protection bridges are nearly gone, but observe that the totally black circuit trench area indicates that trenches are complete, i.e., they form a "V" and no flat reflecting surface on the bottom.

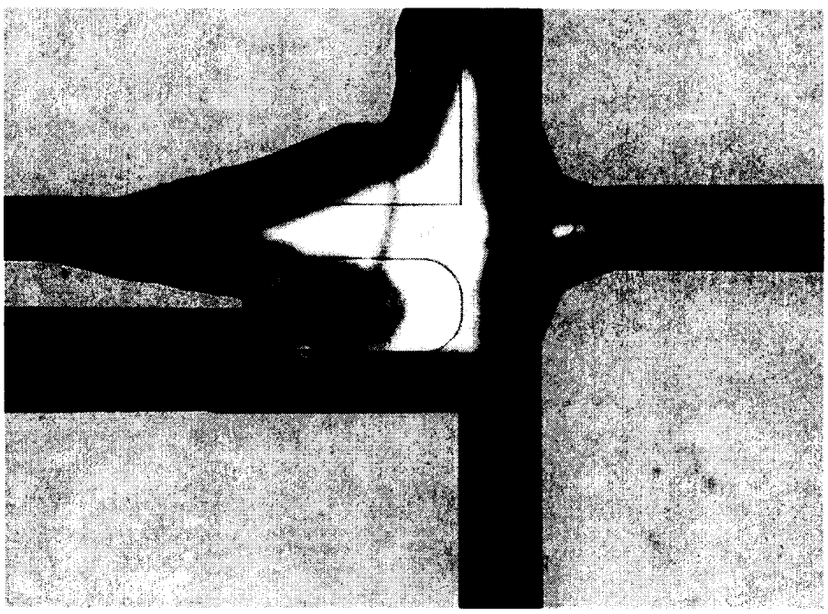

Fig. 16: The EDP etch progression in the same layout area as Fig. 11 after 80 minutes; the spacer trench is complete. The corner protection bridges are gone, but observe minimal undercutting has occurred yet.

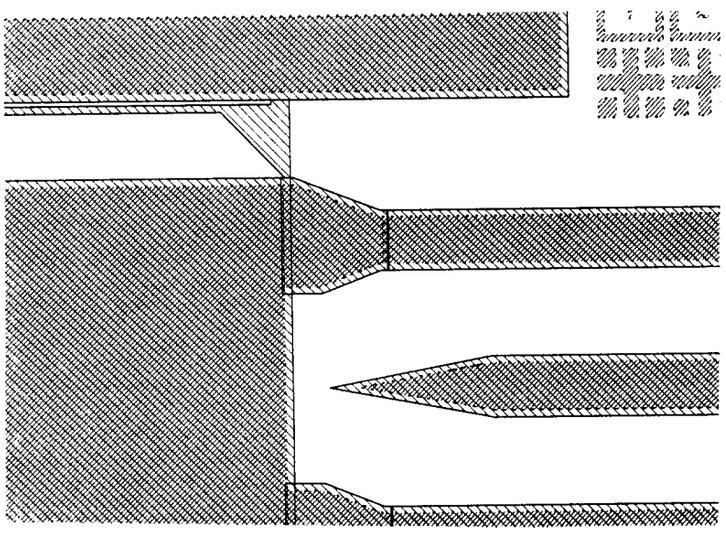

Fig. 17: A blow-up of area 1 of Fig. 12.

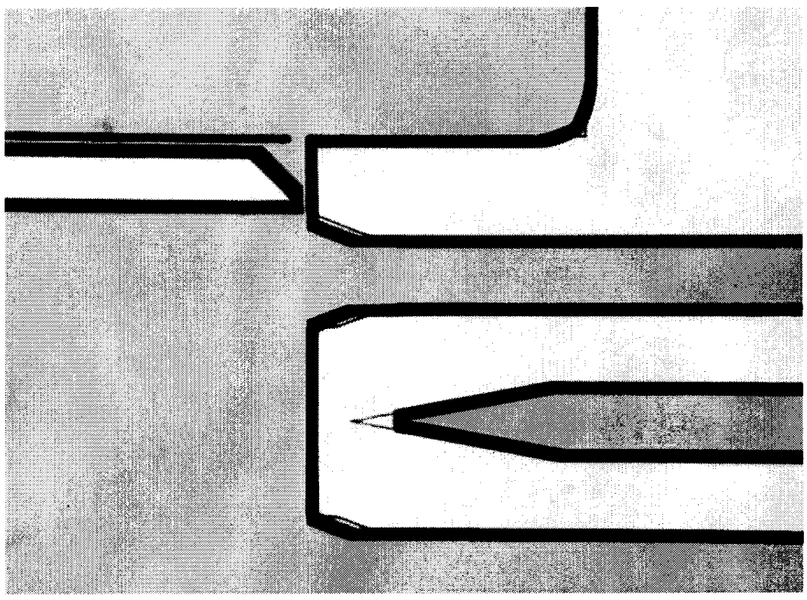

Fig. 18: : The EDP etch progression in the same layout area as Fig. 17 after 20 minutes. The tip of the shank has only begun to undercut a little bit.

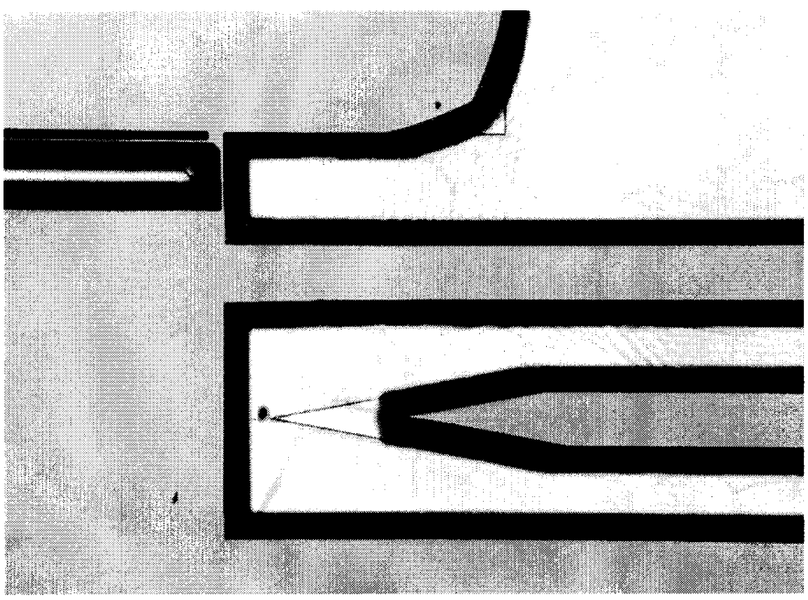

Fig. 19: : The EDP etch progression in the same layout area as Fig. 17 after 40 minutes. The tip of the shank has undercut almost back to the start of the bevel.

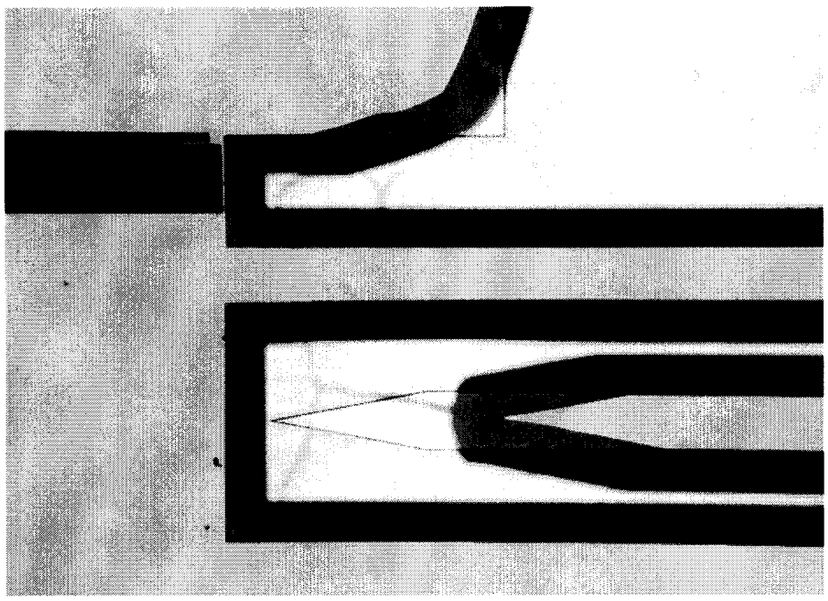

Fig. 20: The EDP etch progression in the same layout area as Fig. 17 after 60 minutes. Note, the circuit area trench has completed.

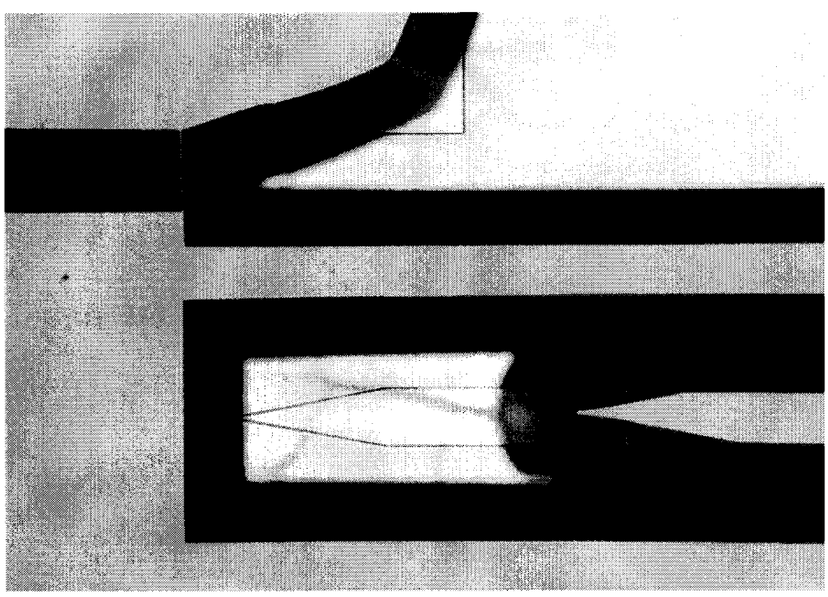

Fig. 21: The EDP etch progression in the same layout area as Fig. 17 after 80 minutes. The shanks have etched back quite a ways, but not nearly enough to release them. Note, the probe corner has not yet been attacked.

In order to observe how the probe etch-out completes, a sample was prepared forming a normal deep boron diffusion and field dielectric with the appropriate masks. The sample was then thinned to 190μm ±10μm and then etched in EDP. Figure 22 shows the shanks etch out very quickly from the backside once the front and back etch planes meet between the shanks. The shanks clear quite quickly while the circuit area still remains quite thick and in no danger of being attacked by EDP. Figure 23 shows a backside photo of a STIM-3B test probe which has been over-etched, yet the circuit area has not been attacked. This is obviously not an ideal etch-out, but it demonstrates that there is a reasonable window for variation in etch-out times.

The etch-out tests are very important in that they have shown the current probes can indeed be successfully etched out without endangering the circuitry. The angled slots in the wings and the bridged corner protection were both very successful in meeting their intended purposes. Iterations of these tests have helped to fine tune the proper thinning time and the proper etch time in EDP.

During the coming quarter, we anticipate completing the fabrication of the STIM-2B and STIM-3B probes. We also plan to completely characterize the probes *in-vitro* and begin performing some *in-vivo* experiments.

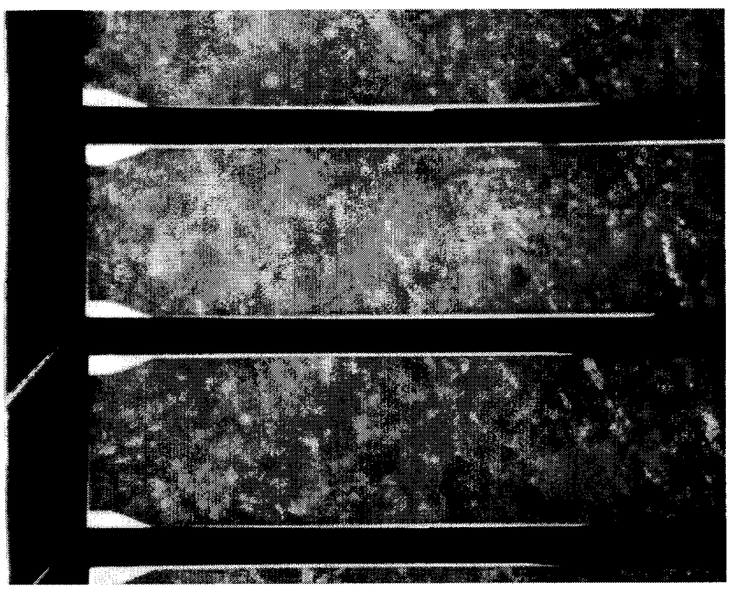

Fig. 22: A back side view of probe shanks which have almost completely cleared while the circuit area is still very thick.

5. Development of External Probe Electronics

We are in the process of constructing and testing a new external electronic system to function as an interface to the upcoming generation of STIM 2b probes. The various design and implementation issues of the system have been presented in previous reports, and they currently remain unchanged. Briefly, the system consists of a DSP-based embedded system comprising a standard serial interface to a host computer, data storage and sequencing devices for generating stimulation control signals and stimulation data, and level conversion and driving logic for the probe interface.

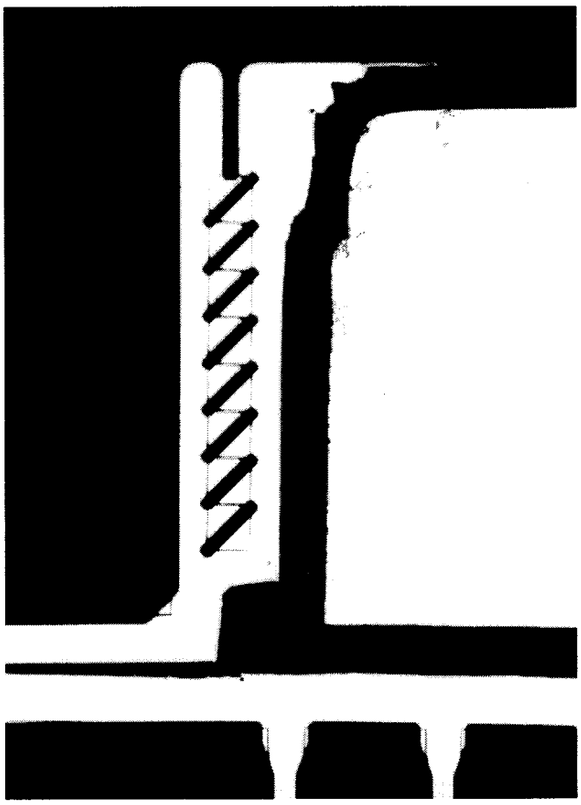

Fig. 23: Photograph of a STIM-3B etch-test probe which has been over-etched, but the circuit area has still not been attacked. The spacer area and shanks have completely cleared.

Our focus during the past quarter has been the completion of simulation and timing waveforms for the design, as well as the realization of the design on a wire-wrap carrier. Both of these tasks are now complete, and we now have a prototype implementation of our new system. As mentioned previously, the prototype will most likely not be able to operate at the maximum designed speed (due to the physical limitations of wire-wrap circuits) nor stimulate at the maximum bit rate of 10 Mbps. We do expect the prototype to be functional, however, so that we may use it to control a STIM 2b probe in a test environment.

The prototype system has been submitted to basic electrical tests and is now ready for more thorough testing. In the upcoming quarter we will test and debug the prototype, as well as write software to allow simple, manual control over stimulation functions. We expect to have our prototype ready for integration testing with the new STIM 2b probes about halfway through the quarter.

6. *Conclusions*

During the past quarter, additional passive stimulating and recording probes have been fabricated for use by investigators nationwide. A new mask set was also prepared to test a variety of site structures fabricated using two and three mask processes. Wafers are now in process to determine the yield and structural integrity of these sites in an effort to standardize on a design that will offer maximum reliability and yield in future probe fabrication. A new sectioning/polishing technique has been developed to allow cross-sections to be obtained at high resolution through these sites so that they can be evaluated in ways not previously possible. Test structures have also been included to allow the optimization of beam lead dimensions and the bonding parameters associated with these lead transfers.

As part of the continuing optimization of the probe process, we are exploring two new technologies that could offer alternatives, or supplemental processes, to the boron diffusion process now used for probe fabrication. Deep high-aspect-ratio dry etching technology now permits aspect ratios of more than 30:1 and could be used to trench around probe patterns to speed, for example, shank etchout (in combination with a boron etch-stop). Sometimes in the past the shanks have cleared too slowly, delaying etch termination and resulting in excessive attack of circuit areas on active probes. A porous silicon process is also being explored. This electrochemical technique allows formation of a very fast etching layer under normal circuit material and could allow an etch-stop to be formed under lightly-doped silicon containing the circuitry at the back of a probe. This would eliminate any critical timing windows in the formation of active probes. Probes are in process using this porous silicon technique.

Active stimulating probes STIM-2B and -3B are continuing in fabrication. New masking techniques for forming the spacer slots on active 3D structures have been verified experimentally as have layout changes to minimize or eliminate lateral attack of the circuit areas on active probes. These layout changes and the associated etching studies have greatly added to our understanding and ability to optimize the process windows associated with 3D active probe fabrication. We expect completed versions of these active probes during the coming quarter along with the new version of external circuitry for interfacing with them.